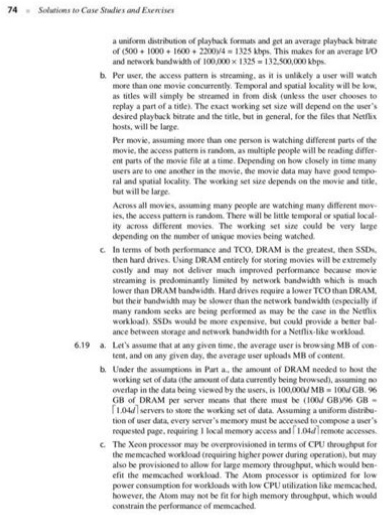

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a uniform distribution of playback formats and get an average playback bitrate of (500 + 1000 + 1600 + 2200)/4 = 1325 kbps. This makes for an average I/O and network bandwidth of 100,000 × 1325 = 132,500,000 kbps.

b. Per user, the access pattern is streaming, as it is unlikely a user will watch more than one movie concurrently. Temporal and spatial locality will be low, as titles will simply be streamed in from disk (unless the user chooses to replay a part of a title). The exact working set size will depend on the user's desired playback bitrate and the title, but in general, for the files that Netflix hosts, will be large.

Per movie, assuming more than one person is watching different parts of the movie, the access pattern is random, as multiple people will be reading different parts of the movie file at a time. Depending on how closely in time many users are to one another in the movie, the movie data may have good temporal and spatial locality. The working set size depends on the movie and title, but will be large.

Across all movies, assuming many people are watching many different movies, the access pattern is random. There will be little temporal or spatial locality across different movies. The working set size could be very large depending on the number of unique movies being watched.

c. In terms of both performance and TCO, DRAM is the greatest, then SSDs, then hard drives. Using DRAM entirely for storing movies will be extremely costly and may not deliver much improved performance because movie streaming is predominantly limited by network bandwidth which is much lower than DRAM bandwidth. Hard drives require a lower TCO than DRAM, but their bandwidth may be slower than the network bandwidth (especially if many random seeks are being performed as may be the case in the Netflix workload). SSDs would be more expensive, but could provide a better balance between storage and network bandwidth for a Netflix-like workload.

6.19 a. Let's assume that at any given time, the average user is browsing MB of content, and on any given day, the average user uploads MB of content.

b. Under the assumptions in Part a., the amount of DRAM needed to host the working set of data (the amount of data currently being browsed), assuming no overlap in the data being viewed by the users, is 100,000*d* MB = 100*d* GB. 96 GB of DRAM per server means that there must be (100*d* GB)/96 GB = ⌈1.04*d*⌉ servers to store the working set of data. Assuming a uniform distribution of user data, every server's memory must be accessed to compose a user's requested page, requiring 1 local memory access and ⌈1.04*d*⌉ remote accesses.

c. The Xeon processor may be overprovisioned in terms of CPU throughput for the memcached workload (requiring higher power during operation), but may also be provisioned to allow for large memory throughput, which would benefit the memcached workload. The Atom processor is optimized for low power consumption for workloads with low CPU utilization like memcached, however, the Atom may not be fit for high memory throughput, which would constrain the performance of memcached.

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With blocking caches, the presence of misses effectively freezes progress\nmade by the machine, so whether there are misses or not doesn\u2019t change the\nrequired number of write buffer entries. If the memory\n\nCopyright \u00a9 2012 Elsevier, Inc. From Figure 2.14, this\nis just barely within the bandwidth provided by DDR2667 DIMMs, so just one\nmemory channel would suffice.\n\na. The system built from 1Gb DRAMs will have twice as many banks as the\nsystem built from 2Gb DRAMSs. Thus the 1Gbbased system should provide\nhigher performance since it can have more banks simultaneously open.\n\nb. The power required to drive the output lines is the same in both cases, but the\nsystem built with the x4 DRAMs would require activating banks on 18 DRAMs,\nversus only 9 DRAMSs for the x8 parts. The page size activated on each x4 and\nx8 part are the same, and take roughly the same activation energy. If the accesses are back to back, then this is not possible. This\nnew constrain will not impact policy 1.\n\nCopyright \u00a9 2012 Elsevier,

Inc. Similar behavior with\ndifferent flattening points on L2 and L3 caches are observed.\n\nb. The IPC decreases by 60%, 20%, and 66% when input data size goes from\n8KB to 128 KB, from 128KB to 4MB, and from 4MB to 32MB, respectively.\nThis shows the importance of all caches. Among all three levels, LI and L3\ncaches are more important. This is because the L2 cache in the Intel\u00ae Xeon\u00ae\nProcessor X5680 is relatively small and slow, with capacity being 256KB and\nlatency being around 11 cycles.\n\nc. For a recent Intel i7 processor 3.3GHz Intel\u00ae Xeon\u00ae Processor X5680,\nwhen the data set size is increased from 8KB to 128KB, the number of L1\nDeache misses per 1K instructions increases by around 300, and the number\nof L2 cache misses per 1K instructions remains negligible.

With a 11 cycle\nmiss penalty, this means that without prefetching or latency tolerance from\noutoforder issue we would expect there to be an extra 3300 cycles per 1K\ninstructions due to L1 misses, which means an increase of 3.3 cycles per\ninstruction on average. All rights reserved.\n\f3.1\n\n3.2\n\nChapter 3 Solutions 13\n\nChapter 3 Solutions\n\nCase Study 1 Exploring the Impact of Microarchitectural\nTechniques\n\nThe baseline performance in cycles, per loop iteration of the code sequence in\nFigure 3.48, if no new instruction\u2019s execution could be initiated until the previ\nous instruction\u2019s execution had completed, is 40. See Figure S.2. Each instruc\ntion requires one clock cycle of execution a clock cycle in which that\ninstruction, and only that instruction, is occupying the execution units; since\nevery instruction must execute, the loop will take at least that many clock\ncycles. To that base number, we add the extra latency cycles. Until that output is ready, no dependent\ninstructions can be executed. So the first LD must stall the next instruction for\nthree clock cycles. The MULTD produces a result for its successor, and therefore\nmust stall 4 more clocks, and so on.\n\nCopyright \u00a9 2012 Elsevier, Inc. Assume\nresults can be immediately forwarded from one execution unit to another, or to itself.\nFurther assume that the only reason an execution pipeline would stall is to observe a\ntrue data dependency. Now how many cycles does the loop require. The answer\nis 22, as shown in Figure S.4. The LD goes first, as before, and the DIVD must wait\nfor it through 4 extra latency cycles. After the DIVD comes the MULTD, which can run\nin the second pipe along with the DIVD, since there\u2019s no dependency between them.\nNote that they both need the same input, F2, and they must both wait on F2\u2019s readi\nness, but there is no constraint between them.

The LD following the MULTD does not\ndepend on the DIVD nor the MULTD, so had this been a superscalarorder3 machine,\n\nCopyright \u00a9 2012 Elsevier, Inc. The loop overhead instructions at the loop\u2019s\nbottom also exhibit some potential for concurrency because they do not depend on.\nany longlatency instructions.\n\nPossible answers\n\n1. All rights reserved.\n\f16 Solutions to Case Studies and Exercises\n\n3.5\n\nLonglatency ops are at highest risk of being passed by a subsequent op. Then update all\nthe sre source registers accordingly, so that true data dependencies are main\ntained. All rights reserved.\n\f18 Solutions to Case Studies and Exercises\n\n3.8 See Figure S.8. The rename table has arbitrary values at clock cycle N \u2014 1. Look at\nthe next two instructions 10 and 1 10 targets the F1 register, and I will write the F4\nregister. This means that in clock cycle N, the rename table will have had its entries 1\nand 4 overwritten with the next available Temp register designators. I0 gets renamed\nfirst, so it gets the first T reg 9. In clock cycle N,\ninstructions I2 and I3 come along; 12 will overwrite F6, and 13 will write FO. This\nmeans the rename table\u2019s entry 6 gets 11 the next available T reg, and rename table\nentry 0 is written to the T reg after that 12. What could go wrong\nwith this. If an interrupt is taken between clock cycles 1 and 4, then the results of the LW\nat cycle 2 will end up in R1, instead of the LW at cycle 1. Bank stalls and ECC stalls will\ncause the same effect\u2014pipes will drain, and the last writer wins, a classic WAW hazard.\nAll other \u201cintermediate\u201d results are lost.\n\n3.11 See Figure S.11. The convention is that an instruction does not enter the execution\nphase until all of its operands are ready. So the first instruction, LW R3,0RO,\nmarches through its first three stages F, D, E but that M stage that comes next\nrequires the usual cycle plus

two more for latency. All rights reserved.

\n\f20\n\nSolutions to Case Studies and Exercises\n\n3.12\n\na. 4 cycles lost to branch overhead. Without bypassing, the results of the SUB\ninstruction are not available until the SUB\u2019s W stage. A dynamic branch predictor\nremembers that when the branch instruction was fetched in the past, it eventu\nally turned out to be a branch, and this branch was taken. So a \u201cpredicted taken\u201d\nwill occur in the same cycle as the branch is fetched, and the next fetch after\nthat will be to the presumed target. It feeds the next ADDD, and ADDD\n3 feeds the SD below. With reg renaming, doesnt have\n3 to wait until the LD of a different F4 has\n3 completed.\n\nSUB R20,R4,Rx\n\nBNZ R20, Loop\n\n \n\nFigure S.12 Instructions in code where register renaming improves performance.\n\nCopyright \u00a9 2012 Elsevier, Inc. All rights reserved.\n\fChapter 3 Solutions 21\n\nb. Think of this exercise from the\nReservation Station\u2019s point of view at any given clock cycle, it can only\n\u201csee\u201d the instructions that were previously written into it, that have not\nalready dispatched. All rights reserved.\n\n \n\fChapter 3 Solutions 23\n\n1. Another ALU 0% improvement\n2. Cutting longest latency in half divider is longest at 12 cycles. IFRS schedules 2nd loops critical LD in cycle 2, then\nloop 2s critical dependency chain will be the same length as loop 1sis. Since were not\nfunctionalunitlimited for this code, only one extra clock cycle is needed.\n\nCopyright \u00a9 2012 Elsevier, Inc. All rights reserved.\n\f24\n\nSolutions to Case Studies and Exercises\n\n3.13\n\nExercises\n\na. All rights reserved.\n\f3.18\n\nChapter 3 Solutions 31\n\nFor this problem we are given the base CPI without branch stalls. Storing the target instruction of an unconditional branch effectively removes\none instruction. If there is a BTB hit in instruction fetch and the target\ninstruction is available, then that instruction is fed into decode in place of the\nbranch instruction.

The penalty is 1 cycle. The hit percentage\nto just break even is simply 20%.\n\nCopyright \u00a9 2012 Elsevier, Inc.All rights reserved.\n\f46\n\nSolutions to Case Studies and Exercises\n\n5.5\n\n56\n\n. pO read 120, Read mi\n\nd. All rights reserved.\n\f57\n\nChapter 5 Solutions 47\n\nd. Assume the processors acquire the lock in order. PO will acquire it first, incur\nring 100 stall cycles to retrieve the block from memory. P1 and P3 will stall\nuntil PO\u2019s critical section ends pingponging the block back and forth 1000\ncycles later. PO will stall for about 40 cycles while it fetches the block to\ninvalidate it; then P1 takes 40 cycles to acquire it. P1\u2019s critical section is 1000\ncycles, plus 40 to handle the write miss at release. Finally, P3 grabs the block\nfor a final 40 cycles of stall. So, PO stalls for 100 cycles to acquire, 10 to give\nit to P1, 40 to release the lock, and a final 10 to hand it off to P1, for a total of\n160 stall cycles. Finally, P3\ngets the lock 40 cycles later, so it stalls a total of 2280 cycles.\n\nb. The optimized spin lock will have many fewer stall cycles than the regular\nspin lock because it spends most of the critical section sitting in a spin loop\nwhich while useless, is not defined as a stall cycle. So approximately 945 cycles total.\n\nc. Approximately 31 interconnect transactions. The first processor to win arbi\ntration for the interconnect gets the block on its first try 1; the other two\npingpong the block back and forth during the critical section. Because the\nlatency is 40 cycles, this will occur about 25 times 25. The first processor\ndoes a write to release the lock, causing another bus transaction 1, and the\nsecond processor does a transaction to perform its test and set 1. The last\nprocessor gets the block 1 and spins on it until the second processor releases\nit 1. Finally the last processor grabs the block 1.\n\nCopyright \u00a9 2012 Elsevier, Inc. All rights reserved.

\n\f48\n\nSolutions to Case Studies and Exercises\n\nd. Approximately 15 interconnect transactions. Assume processors acquire the\nlock in order. All three processors do a test, causing a read miss, then a test\nand set, causing the first processor to upgrade and the other two to write\nmiss 6. The losers sit in the test loop, and one of them needs to get back a\nshared block first 1. When the first processor releases the lock, it takes a\nwrite miss 1 and then the two losers take read misses 2. Both have their\ntest succeed, so the new winner does an upgrade and the new loser takes a\nwrite miss

2. The loser spins on an exclusive block until the winner releases\nthe lock 1. The loser first tests the block 1 and then testandsets it, which\nrequires an upgrade 1.\n\n5.8 Latencies in implementation 1 of Figure 5.36 are used.\n\n59\n\na. PO write 110 \u20ac 80\nPO read 108\nb. PO write 100 \u20ac 80\n\nPO read 108\n\nc. PO write 110 \u20ac 80\nPO write 100 \u20ac 90\n\nd. All rights reserved.\n\fChapter 5 Solutions 49\n\n5.10 a. PO,0 write 100 \u20ac 80, Write hit only seen by PO,0\n\nb. PO0,0 write 108 \u00a9 88, Write \u201cupgrade\u201d received by P0,0; invalidate received\nby P3,1\n\nc. PO,0 write 118 \u00a9 90, Write miss received by PO,0; invalidate received by P1,0\nd. It also allows silent downgrades to I,\nallowing the processor to discard its copy with notifying memory. The memory\nmust have a way of inferring either of these transitions. In a directorybased system,\nthis is typically done by having the directory assume that the node is in state M and\nforwarding all misses to that node. If a node has silently downgraded to I, then it\nsends a NACK Negative Acknowledgment back to the directory, which then\ninfers that the downgrade occurred. However, this results in a race with other mes\nsages, which can cause other problems.\n\nCopyright \u00a9 2012 Elsevier, Inc. PO,0 read 100 Read hit, 1 cycle\n\nb.

It is crucial that the protocol implementation guarantee at least with a\nprobabilistic argument that a processor will be able to perform at least one mem\nory operation each time it completes a cache miss. Otherwise, starvation might\nresult. If a processor is not guaranteed to be able to perform at least one\ninstruction, then each could steal the block from the other repeatedly. In the worst\ncase, no processor could ever successfully perform the exchange.\n\nCopyright \u00a9 2012 Elsevier, Inc. All rights reserved.\n\f5.18\n\n5.20\n\nChapter 5 Solutions 53\n\na. P1,0 read 100\nP3,1 write 100 \u20ac 90\n\nIn this problem, both P0,1 and P3,1 miss and send requests that race to the\ndirectory. Assuming that PO,1\u2019s GetS request arrives first, the directory will\nforward PO,1\u2019s GetS to P0,0, followed shortly afterwards by P3,1\u2019s GetM. If\nthe network maintains pointtopoint order, then P0,0 will see the requests in\nthe right order and the protocol will work as expected. That latter number depends on both the topology and the application.\n\nc. Since the CPU frequency and the number of instructions executed did not\nchange, the answer can be obtained by the CPI for each of the topologies\nworst case or average by the base no remote communication CPI.\n\nTo keep the figures from becoming cluttered, the coherence protocol is split into\ntwo parts as was done in Figure 5.6 in the text. Figure S.34 presents the\nCPU portion of the coherence protocol, and Figure S.35 presents the bus portion\nof the protocol. In both of these figures, the arcs indicate transitions and the text\nalong each arc indicates the stimulus in normal text and bus action in bold text\nthat occurs during the transition between states. Finally, like the text, we assume a\nwrite hit is handled as a write miss.\n\nFigure S.34 presents the behavior of state transitions caused by the CPU itself.